We claim:

1. A method of operating a phase-change memory element, said memory element including a phase-change material, said method comprising:

providing said phase-change memory element including said phase-change material; and

programming said phase-change memory element from a first memory state having a first threshold voltage to a second memory state having a second threshold voltage.

2. The method of claim 1, wherein said phase-change material is in the amorphous phase in said first memory state and said second memory state.

3. The method of claim 1, wherein said phase-change material is in a saturated condition in said first memory state and said second memory state.

4. The method of claim 1, wherein said phase-change material includes a chalcogen element.

5. A method of operating a phase-change memory element, said memory element comprising a phase-change material, said method comprising:

providing said phase-change memory element including said phase-change material; and

programming said phase-change memory element from a first memory state to a second memory state, said phase-change material being in the amorphous phase in said first memory state and said second memory state.

6. The method of claim 5 wherein said phase-change material includes a chalcogen element.

7. A method of reading the current memory state of a phase-change memory element including a phase-change material, said phase-change memory element having at least a first memory state with a first threshold voltage and a second memory state with a second threshold voltage, said method comprising:

providing said phase-change memory element including said phase-change material; and

using said first threshold voltage and said second threshold voltage to determine the current memory state of said phase-change memory element.

8. The method of claim 7, wherein said phase-change material includes a chalcogen element.

9. An electrically programmable memory element having a plurality of memory states, comprising:

a phase-change material, said phase-change material being in the amorphous phase in each of said memory states.

10. The memory element of claim 9, wherein each of said memory states has a corresponding threshold voltage.

11. The memory element of claim 9, wherein said phase-change material includes a chalcogen element.

12. An electrically programmable memory array, comprising:

a row line;

a column line; and

a memory element coupled to said row line and said column line, said memory element having at least a first memory state and a second memory state, said memory element including a phase-change material, said phase-change material being in the amorphous phase in said first memory state and in said second memory

state.

13. The memory array of claim 12, wherein said memory element is coupled to said row line or said column line through an isolation device.

14. The memory array of claim 12, wherein said isolation device is selected from the group consisting of diode and transistor.

15. The memory array of claim 12, wherein each of said first memory state has a first threshold voltage and said second memory state has a second threshold voltage.

16. The memory element of claim 12, wherein said phase-change material includes a chalcogen element.

17. An electrically programmable memory element having at least a first memory state and a second memory state, comprising:

a phase-change material wherein said first memory state has a first threshold voltage and said second memory state has a second threshold voltage.

18. The memory element of claim 17, wherein said phase-change material is in a saturated condition in said first memory state and said second memory state.

19. The memory element of claim 17, wherein said phase-change material includes a chalcogen element.

20. An electrically programmable memory array, comprising:

a row line;

a column line; and

a memory element including a phase-change material, said memory element coupled to said row line and said column line, said memory element having at least a

first memory state with a first threshold voltage and a second memory state with a second threshold voltage.

21. The memory array of claim 20, wherein said memory element is coupled to said row line or said column line through an isolation device.

22. The memory array of claim 20, wherein said isolation device is selected from the group consisting of diode and transistor.

23. The memory array of claim 20, wherein said phase-change material is in a saturated condition in said first memory state and said second memory state.

24. The memory element of claim 20, wherein said phase-change material includes a chalcogen element.